**CECS 341 - Lab 1**

**“ALU Structural Model”**

**Due date: 01/29/19**

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I certify that this submission is my original work

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Lab Report: Lab Assignment 1 - “ALU Structural Model”

1. **Goal:** The goal of this lab is to model specific operations of the Arithmetic Logic Unit (ALU) using structural Verilog.
2. **Steps:**
   1. Step 1 was to copy the test bench over to the current lab.
   2. Step 2 was to copy the skeleton code for the design file.
   3. Step 3 is to determine the syntax necessary for understanding Table 1.1 in the lab using Verilog.
   4. Step 4 complete the skeleton code in the design file of the lab, complete each case to match each ALU operation from Table 1.1.
   5. Step 5 was to check each of the test cases by hand to determine that the program was working correctly.
   6. Step 6 was to comment what each part of the design did to better understand to ALU process.
3. **Results:** The results of the lab were nine different test cases of each ALU operation. The output will display the test case number, the ALU operation code, the a and b input, the y output, and the carry, negative, zero, and parity flags. Total of 71 test cases.
4. **Conclusion:** I learned how each of the given ALU operations worked in Verilog. The challenge I ran into was determining the syntax needed for the XOR, and SHL operations.